UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,930	01/13/2005	Tommi Koistinen	60282.00238	7618

32294 7590 06/03/2008

SQUIRE, SANDERS & DEMPSEY L.L.P.
8000 TOWERS CRESCENT DRIVE
14TH FLOOR
VIENNA, VA 22182-6212

EXAMINER	
TAHA, SHAQ	

ART UNIT	PAPER NUMBER
2146	

MAIL DATE	DELIVERY MODE
06/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,930	KOISTINEN ET AL.	
	Examiner	Art Unit	
	SHAQ TAHA	2146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 26 - 37, 41 - 56 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 26 - 37, 41 - 56 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a final action for application number 10/518,930 based on after non-final filed on 11/20/2007. The original application was filed on 12/27/2004. Claims 26 – 37, 41 - 56 are currently pending and have been considered below. Claims 26, 41, 50, 51, 52, 53, and 54 are independent claims.

Response to Arguments

Applicant's arguments with respect to claims 26 – 37, and 41 - 56have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

- Claims 26 – 37, and 41 - 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6.272.522) in view of Pham et al. (US 2003/00744388).

Regarding claims 26, 41, 44, and 50 - 54, Lin et al. teaches a method, comprising: obtaining a current connection state as well as a current load state of each of a plurality

of processors configured to perform communication in a packet switched connection from data storage, **[Fig. 7, Ref # 10, wherein the load balancing and packet switching device 10 remain continuously in an operational state, wherein the state of the connection and current load are always in an operational state, (Col. 8, line 18);**

Lin et al. further teaches maintaining information about the load state of each processor so that said selecting is performed by selecting one of said processors to serve and process a respective packet based on the load state, **[Fig. 4, Ref # 58, wherein routing daemon 58 within the control processor 42 is a program that executes in the background to retrieve the information stored in the routing table 62 and maintains the status of the routing table 62 as changes are made to the configuration, which selects the processor depending on the current load state, (Col. 6, Line 63)];**

Lin et al. differs from the claimed invention is that selecting per packet a processor to distribute the next packet to the processor with the lowest load is not taught by Lin et al.

Pham et al. teaches a Load balanced scalable network gateway processor architecture.

Pham et al. further teaches selecting on a per packet basis, by a load balancer configured to distribute load to said balancing unit processors, a processor in such a manner that a respective next packet is distributed to one of said processors having a lowest load irrespective of a specific connection to which this next packet belongs, **[Fig. 10, Ref # 180, The ingress processor distributes inbound data packets to the compute processors based on a least load value selected from current load**

values determined for the respective compute processors of the scalable array, (Abstract)];

Regarding claim 44, Pham teaches an apparatus wherein a load state of a processor is expressed as value which corresponds to the percentage of load, **[The lower bound may be simply determined as a fixed percentage of the FIFO depth, such as 10%, or a size dependent on the time necessary for the crypto processor 86 to process one typical data packet, (Paragraph 0057)].**

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Lin et al. by including that selecting on a per packet basis, a processor in such a manner that a respective next packet is distributed to one of said processors having a lowest load irrespective of a specific connection to which this next packet belongs as taught by Pham et al.

One of ordinary skill in the art would have been motivated to make this modification in order provide the advantage of a processor distributing said inbound data packet to said scalable array of compute processors based on a least load value selected from current load values determined for the respective compute processors of said scalable array of compute processors.

Regarding claim 27, Lin teaches an apparatus, wherein said data storage is accessed by said load balancer load balancing unit, **[Fig. 8, Ref # 68, wherein shared memory is accessed by control processor 42 in load balancer 10].**

Regarding claim 28, Lin teaches an apparatus, wherein said data storage is accessed by said processors, **[Fig. 8, Ref # 68, wherein shared memory is accessed by control processor 42].**

Regarding claims 29, 43, Lin teaches an apparatus, wherein said information about the load state is maintained as a Boolean state, **[it is inherent to use a Boolean value, since it is a digital or analog that depends on 1s and 0s, or true and false].**

Regarding claim 30, Lin teaches an apparatus, wherein a processor is selected in a round-robin fashion, **[it is inherent to use a round-robin fashion, since it is describes correspondence authored or signed by numerous individuals to a single address].**

Regarding claim 31, Lin teaches a method, wherein a supported service profile for each unit processor is maintained, **[Fig. 7, Ref # 44, wherein the processor maintains its own service profile].**

Regarding claim 32, Lin teaches a method, wherein said supported service profile is used as additional selection criteria, **[The switching processors route received ones of the data packets to a selected one of the external networks in accordance with information included in a header portion of the data packets and the load distribution configuration data, (Abstract)].**

Regarding claim 33, Lin teaches a method, wherein said load balancer is configured to obtain a load state from each processor upon a hardware based mechanism, **[The operating system level, provides the basic services for the control processor 42 as well as the switching processor 44, such as activating the hardware directly, (Col. 8, Line 54)].**

Regarding claim 34, Lin teaches an apparatus, wherein said load balancer balancing unit is configured to obtain a load state from each processor upon a packet based mechanism, **[The switching processor 44 obtains the current load distribution data from the active buffer, (Col. 7, line 12)].**

Regarding claim 35, Lin teaches a method, wherein a load state of processor is inserted into a packet processed by said processor, **[the switching processors re-write the routing information included in the header portion of the data packets to reflect the selected one of the external networks, (Abstract)].**

Regarding claim 36, Lin teaches a method, wherein a packet returned by a processor is interpreted as a flag for a free resource, **[Fig. 4, Ref # 74, wherein the packet is returned by the packet filter and considered as flag].**

Regarding claim 37, 49 and 56, Lin teaches a method, wherein excess traffic is redirected to another load balancer, said excess traffic being defined upon the number of active processors, **[Fig. 1, Ref # 6, wherein traffic is routed to a new load balancer, [Routers read the network address in each transmitted data packet and make a decision on how to send it based on the most expedient route (traffic load, line costs, speed, bad lines, etc.), (Column 4, lines 43 – 46)].**

Regarding claims 42 and 46, Lin teaches an apparatus, wherein a load state of a processor is contained in a table, **[The shared memory further includes a routing table, a configuration table, and a connection table, (Column 6, lines 55 – 56)].**

Regarding claim 45, Lin teaches an apparatus, wherein said selection circuitry is configured such that a processor is selected also on the basis of a parameter indicating the service profile supported by a respective processor, **[Fig. 7, Ref # 44, wherein the processor maintains its own service profile and selected based on parameter indicating the service profile].**

Regarding claims 47 and 55, Lin et al. teaches an apparatus, further comprising data insertion circuitry configured to insert a communication connection state into a packet to be routed, **[the routing table 62 defines the addresses and interconnection pathways between the load balancing and packet switching device 10 and the**

networks connected thereto, (Col. 6, Line 60)].

Regarding claim 48, Lin et al. teaches an apparatus, wherein the processors are comprised of multi core digital signal processing elements having a shared data storage for all cores, whereby said device comprises a first level of load balancing for selecting a digital signal processing means and a second level of load balancing for selecting a single core, **[FIG. 10 is a block diagram illustrating a third embodiment of the invention having a user-level network interface for applications operating on the switching processor, (Column 3, lines 53 – 55)].**

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Shaq Taha** whose telephone number is 571-270-1921. The examiner can normally be reached on 8:30am-5pm Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jeff Pwu** can be reached on 571-272-6798.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shaq Taha

05/30/2008

/Jeffrey Pwu/

Supervisory Patent Examiner, Art Unit 2146